

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)

Martin VORBACH et al.

Serial No.

08/947,254

Filing Date

October 8, 1997

For

I/O AND MEMORY BUS SYSTEM FOR DFPS  
AND UNITS WITH TWO- OR MULTI-  
DIMENSIONAL PROGRAMMABLE CELL  
ARCHITECTURES

Group Art Unit : 2818

Examiner : G. Ray

Assistant Commissioner  
for Patents  
Washington, D.C. 20231

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AMENDMENT

SIR:

This paper addresses the Office Action dated July 20, 1999. Initially, please amend the above-identified application as set forth below.

IN THE CLAIMS:

Please cancel, without prejudice, claims 19 and 20.

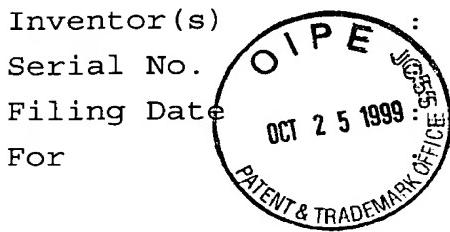
Please amend the claims as follows.

21. (Amended) [The] A bus system [of claim 20], [further] comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture;

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the first plurality of individual lines to form the bus system, the first plurality of individual lines providing communication, via the at least one interface unit, between



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

20 Oct 1999

  
Michelle M. Carniaux (Reg. No. 36.098)

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